REMARKS

Claims 1-3, 6, 10-13, 16-24, 26, 28-33 and 35-37 are pending. Claims 1, 10, 28, and 35 are amended. Claims 4, 7-9, 14, 25, 27, and 34 have been cancelled in a previous amendment.

Applicants acknowledge and thank the Examiner indicating that claims 28-31 contain allowable subject matter, and would be allowed if written in independent form including all the limitation of base claim and any intervening claims.

CLAIM OBJECTIONS

Claims 1-3, 5-6, 15-16 and 35 are objected to because of informalities.

Applicants have amended claims 1, 15 and 35 per the Examiner's suggestion. Withdrawal of this objection is requested in view of the amendments.

CLAIM REJECTIONS 35 USC 112

Claims 1-3, 5-6, 10-13, 15-18, 28-33 and 35-37 are rejected under 35 USC 112, second paragraph as being indefinite. Applicants traverse this rejection.

The Examiner alleges that "operating at a first voltage higher than a power supply voltage of the device" and "operating at a second voltage lower than the first voltage" recited in claim 1 is misleading and/or confusing. Applicants disagree.

It is generally understood that claims should be read with respect to the specification. Accordingly, the specification on paragraph [0021] provides:

> [0021] The NMOS transistor MN1 of the interface circuit 16 prevents a high voltage supplied through a PMOS transistor MP1 from being directly applied to the drain of the NMOS transistor MN2. That is, since a voltage of the output terminal OUT is transferred through the NMOS transistor MN1 (whose gate is coupled to the IVC/EVC voltage), a voltage of IVC/EVC-Vtn1 instead of the high voltage VPP is applied to the drain of the NMOS transistor MN2,

> where Vtn1 denotes a threshold voltage of an NMOS transistor having a relatively thin gate insulation layer. Since the IVC/EVC is always applied to the gate of the NMOS transistor MN1, a gate-drain voltage difference of the NMOS transistor MN1 is VPP-IVC/EVC. Therefore, although the NMOS transistor MN1 has the relatively thin gate insulation layer, a gate insulation layer of the NMOS transistor MN1 is not broken by the high voltage VPP. (Emphasis added.)

In other words, regardless of whether a first voltage VPP is supplied from a first internal circuit through a gate or a source of a transistor MP1, a second voltage IVC/EVC lower than the first voltage will be applied to a second internal circuit by a restricting means. As also disclosed in paragraph [0016], the internal supply voltage IVC is equal to or less than the external supply voltage, but regardless, the voltage of the IVC/EVC is less than the first voltage. Applicants submit that claim 1 is not indefinite.

With regard to claim 6, the Examiner alleges that the recitation that "each PMOS and NMOS transistor operating at a third voltage higher than the power supply voltage" needs clarification.

First, claim 6 is dependent on claim 5. Claim 5 recites an inverter. Claim 5 is broad enough to read that the inverter may or my not include transistors. However, if claim 5 may be read to mean that the inverter includes transistors, then the transistors may operate at either a voltage higher or lower than the power supply voltage. Claim 6 further defines claim 5. Claim 6 specifically recites that the inverter of claim 5 includes a PMOS and an NMOS transistors and that the transistors operate at a voltage higher than the power supply voltage. Since claim 6 is not restricted to an operation at either continuous or selective nature, a lack of such restriction does not render claim 6 misleading and/or confusing.

With respect to claim 10, the Examiner basically alleges that claim 10 may be broad enough to mean a terminal may receive a high voltage continuously or selectively. However, a claim is commonly drafted so that a recitation may have more than one possible definition, function, use, etc. For example, it is common to draft a claim using a Markush group. In a

Markush claim, an element may be one of several elements without the claim being indefinite. Claim 10 is silent on whether a terminal receives a high voltage continuously or selectively, and silence in a claim is not necessarily misleading and/or confusing.

The remarks presented with respect to the rejection of claims 6 and 10 also apply to claims 16 and 31.

Claim 28 has been amended to be consistent with the recitation of claim 19.

The remarks presented with respect to the rejection of claim 1 also apply to claim 32.

With reference to the remarks above, Applicants request the Examiner to withdrawal his §112, second paragraph rejection.

CLAIM REJECTIONS 35 USC 103

Claims 1-3, 5-6, 10-13, 15-18, 32-33 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over Hardee in view of Origasa. Applicants traverse this rejection.

The Examiner alleges that Origasa teaches a memory device that utilizes a level shifter. The Examiner further alleges that it would have been obvious to couple an inverter to drive a word line of a memory device taught by Origasa.

Without acquiescing to the Examiner's allegations, Applicants submit that Origasa is not proper prior art. The earliest US filing date of Origasa under §102(e) is **May 1, 2003**. The present application claims priority under 35 U.S.C. 119 to Korean Patent Application No. 10-2003-0008200 filed on **February 10, 2003**. Accordingly, Origasa is not prior art. Applicants submit herewith an English translation of Korean Patent Application No. 10-2003-0008200 filed on February 10, 2003 along with a Statement of Accurate Translation.

For at least the reasons given above, Applicants submit that independent claims 1, 10 and 32 are patentable over Hardee in view of Origasa. Dependent claims 2-3, 6, 11-13, 16-18, 33 and 35-37 are also patentable for respectively depending on an allowable case claim.

Claims 1-3, 5-6, 10-13, 15-16, 19-24, 26, 32-33 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over Origasa in view of Wright et al. Applicants traverse this rejection.

Applicants do not acquiesce to the Examiner's allegation, however, Origasa is not proper prior art. The earliest US filing date of Origasa under §102(e) is **May 1, 2003**. The present application claims priority under 35 U.S.C. 119 to Korean Patent Application No. 10-2003-0008200 filed on **February 10, 2003**. Accordingly, Origasa is not prior art.

For at least the reasons given above, Applicants submit that independent claims 1, 10, 19 and 32 are patentable over Origasa in view of Wright et al. Dependent claims 2-3, 6, 11-13, 16-20-24, 26, 33 and 35-37 are also patentable for respectively depending on an allowable case claim.

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CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-3, 5, 6, 10-13, 15-24, 26, 28-33 and 35-37 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

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Attachments: Statement of Accurate Translation
English Translation of Korean Patent Application No. 10-2003-0008200, filed February 10, 2003